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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,045	12/31/2001	Hahn Vo	H052617.1142US0	2278

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EXAMINER	
LI, ZHUO H	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 08/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,045	VO, HAHN	
	Examiner	Art Unit	
	Zhuo H. Li	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is in response to the amendment filed 5/17/2004 (paper no. 6).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-12, 14-21 and 34-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vartti et al. (US PAT. 5,678,026 hereinafter Vartti) in view of Hanawa et al. (US PAT. 5,740,401 hereinafter Hanawa).

Regarding claim 1, Vartti discloses a method of controlling access to a shared memory (10, figure 1) of a multiprocessor system, the multiprocessor system comprising a first bus (I/O SUBSYS 1, figure 1) and a second bus (I/O SUBSYS 2, figure 1) coupled to the shared memory, the first bus coupled to a first processor (IP1, figure 1) and the second bus coupled to a second processor (IP5, figure 1) comprising requesting exclusive access to a first memory location of the sheared memory by the first processor (col. 6 lines 38-54) and granting exclusive access to the first memory location of the shared memory to the first processor (col. 6 lines 54-62). Although Vartti teaches to locks may be granted in parallel if there are not conflicting lock request, Vartti

does not specifically teaches to allow access to a second memory location of the shared memory to the second processor while the first processor has exclusive to the first memory location. However, Hanawa discloses a method of controlling access to a shared memory (130 and 140, figure 1) of a multiprocessor system comprising the steps of requesting exclusive access to a first memory location of the shared memory by the first processor, , and allowing accessing to a second memory location of the shared memory to the second processor while the first processor had exclusive access to the first memory location (abstract, col. 2 lines 15-45 and col. 11 line 52 through col. 13 line 45), in order to improve the throughput by processing memory accesses to different memory banks in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Vartti in allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive to the first memory location, as per teaching of Hanawa, in order to improve the throughput by processing memory accesses to different memory banks in parallel.

Regarding claim 2, Hanawa discloses to request exclusive access by asserting a lock signal on the first bus and sending a lock request from the first processor (110, figure 1) to a memory controller (500, figure 1) coupled to the first bus, the second bus, and the shared memory (col. 11 line 62 through col. 12 line 7).

Regarding claim 4, Hanawa teaches to forward the lock request from the memory controller to a switch (506, figure 7), and signaling the first processor to retry the lock request (col. 13 line 61 through col. 14 line 6).

Regarding claims 5-6, Hanawa teaches to grant exclusive access by signaling the memory controller by the switch to retry the lock request (col. 13 line 61 through col. 14 line 6), assigning

exclusive access to the first memory location by the switch by determining if the first memory location is currently assigned, saving a lock request information if the first memory location is not currently assigned and sending the lock request information to the memory controller (col. 14 lines 14-51), notifying the memory controller of the exclusive access assigned in the assigning step and granting exclusive access to the first memory location by the memory controller responsive to a retry of the lock request by the first processor (col. 14 liens 51-67).

Regarding claims 7-8, Vartti discloses the lock request information comprising a node ID of the first processor, a cycle ID, i.e., directory ID of the first processor and a memory address data for a first memory location (col. 10 line 59 through col. 11 line 64).

Regarding claim 9, Vartti teaches to release exclusive access to the first memory location (col. 8 lines 9-16).

Regarding claim 10, the limitation of the claim is rejected as the same reasons set forth in claim 1.

Regarding claim 11, the limitation of the claim is rejected as the same reasons set forth in claims 2 and 4.

Regarding claim 12, Vartti discloses the shared memory comprising memory subsystem 1 coupled to first storage controller and memory subsystem 2 coupled to a second storage controller of a different multiprocessor node of the plurality of multiprocessor nodes (figure 1).

Regarding claims 14-15, Hanawa discloses the first memory address data referencing the first memory (130, figure 1) or the second memory and the second memory address referencing the second memory (140, figure 1) or the first memory (col. 5 lines 39-45 and col. 7 lines 53-63).

Regarding claim 16, the limitation of the claim is rejected as the same reasons set forth in claim 4.

Regarding claims 17-18, the limitation of the claims is rejected as the same reasons set forth in claims 5-6.

Regarding claims 19, the limitation of the claim is rejected as the same reasons set forth in claims 7-8.

Regarding claim 20, the limitation of the claim is rejected as the same reasons set forth in claim 9.

Regarding claim 21, Vartti discloses a computer system for utilizing a shared memory (10, figure 1) comprising a first multiprocessor node comprising a first processor bus (52, figure 1), a first processor (IP 1, figure 1) coupled to the first processor bus comprising circuityry to generate an exclusive access request for a first memory location, a second processor bus (54, figure 1), a second processor coupled to the second processor bus to request access to second memory location, a first memory (memory subsys 1, figure 1), a first memory controller (storage controller 1, figure 1) coupled to the first processor bus, the second processor bus and the first memory, wherein the first memory controller is adapted to allow exclusive access to the first memory location by the first processor (col. 6 lines 38-62). Although Vartti teaches to locks may be granted in parallel if there are not conflicting lock request, Vartti does not specifically teaches to allow access to a second memory location of the shared memory to the second processor while the first processor has exclusive to the first memory location. However, Hanawa discloses a method of controlling access to a shared memory (130 and 140, figure 1) of a multiprocessor system comprising the steps of requesting exclusive access to a first memory location of the

shared memory by the first processor, and allowing accessing to a second memory location of the shared memory to the second processor while the first processor had exclusive access to the first memory location (abstract, col. 2 lines 15-45 and col. 11 line 52 through col. 13 line 45), in order to improve the throughput by processing memory accesses to different memory banks in parallel. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Vartti in allowing access to a second memory location of the shared memory to the second processor while the first processor has exclusive to the first memory location, as per teaching of Hanawa, in order to improve the throughput by processing memory accesses to different memory banks in parallel.

Regarding claim 34, the limitation of the claim is rejected as the same reasons set forth in claims 2 and 4.

Regarding claim 35, Varrti teaches each of the first memory controller and the second memory controller storing the lock request information (col. 7 lines 36-55).

Regarding claim 36, Hanawa teaches the memory controller storing switch request information in respective register in the memory controller (col. 6 lines 7-39).

4. Claims 3 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vartti et al. (US PAT. 5,678,026 hereinafter Vartti) in view of Hanawa et al. (US PAT. 5,740,401 hereinafter Hanawa) in view of Schibinger et al. (US PAT. 6,092,156 hereinafter Schibinger).

Regarding claim 3, the combination of Vartti and Hawana differs from the claimed invention in not specifically teaching to assert a lock signal by asserting a split lock signal on the first bus, wherein the split lock signal indicating that the lock request contains two memory

address data. However, Schibinger teaches a method for avoiding deadlocks utilizing split lock operation to provide exclusive access to memory by asserting a split lock signal on a bus (520, figure 5), wherein the split lock signal indicating that the lock request contains more than one cache line (col. 8 lines 17-34). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Vartti and Hawana in asserting the split lock signal on the first bus, wherein the split lock signal indicating that the lock request contains two memory address data, as per teaching of Schibinger, in order to provide exclusive access to memory for avoiding deadlocks.

Regarding claim 13, the limitations of the claim are rejected as the same reasons set forth in claim3.

Allowable Subject Matter

5. Claims 22-33 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments with respect to claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Satou et al. (US PAT. 6,101,584) discloses a computer system including a memory and central processing unit for making interlock access to the memory (abstract).

Shagam (US PAT. 5,987,550) discloses a lock mechanism for shared resources in data processing system (abstract).

Tsuchiva et al. (US PAT. 5,408,629) discloses a method for controlling exclusive access to addressable memory in a multiprocessor system (abstract).

8. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7238

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li
Art Unit 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100